AMENDMENTS TO THE CLAIMS:

If entered, this listing of claims will replace all prior versions and listings of claims in the application.

Listing of Claims:

1. (Currently Amended) A method of forming self-aligned, anti-via interconnects in an integrated circuit device comprising:

providing a semiconductor substrate;

depositing a first metal layer overlying said semiconductor substrate;

depositing an etch stop layer overlying said first metal layer wherein said etch stop layer comprises a tungsten containing film;

depositing a second metal layer overlying said etch stop layer;

depositing an anti-reflective coating layer comprising titanium nitride overlying said second metal layer;

etching through said second metal layer, said etch stop layer, and said first metal layer to form connective lines;

thereafter etching through said second metal layer to form vias;

thereafter depositing a dielectric layer overlying said vias, said connective lines and said semiconductor substrate ~~wherein said dielectric layer is SiOF (fluorinated silica glass), SiOC (C-substituted siloxane), amorphous SiC:H, MSQ (methylsilsesquioxane), porous materials, PPXC polymer (poly(chloro-p-xylylene), PPXN polymer (poly-p-xylylene), or VT-4 (tetrafluoro-p-xylylene)~~; and

polishing down said dielectric layer to complete said self-aligned, anti-via interconnects in the manufacture of the integrated circuit device.

2. (Previously Presented) The method according to Claim 1 wherein said first and second metal layers comprise one of the group of: aluminum, aluminum alloys, tungsten and copper.

3. (Original) The method according to Claim 1 wherein said semiconductor substrate comprises semiconductor devices in and on a silicon substrate covered by an insulating layer.

4. (Canceled)

5. (Canceled)

6. (Original) The method according to Claim 1 wherein said dielectric layer is deposited to a thickness of between about 5,000 Angstroms and 20,000 Angstroms.

7. (Canceled)

8. (Canceled)

9. (Currently Amended) A method of forming self-aligned, anti-via interconnects in an integrated circuit device comprising:

providing a semiconductor substrate;

depositing a first metal layer overlying said semiconductor substrate;

depositing an etch stop layer overlying said first metal layer wherein said etch stop layer comprises a tantalum containing film;

depositing a second metal layer overlying said etch stop layer;

<u>depositing an anti-reflective coating layer comprising titanium nitride overlying said second metal layer;</u>

etching through said second metal layer, said etch stop layer, and said first metal layer to form connective lines;

thereafter etching through said second metal layer to form vias;

thereafter depositing a dielectric layer overlying said vias, said connective lines and said semiconductor substrate wherein said dielectric layer is SiOF (fluorinated silica glass), SiOC (C-substituted siloxane), amorphous SiC:H, MSQ (methylsilsesquioxane), porous materials, PPXC polymer (poly(chloro-p-xylylene), PPXN polymer (poly-p-xylylene), or VT-4 (tetrafluoro-p-xylylene); and

polishing down said dielectric layer to complete said self-aligned, anti-via interconnects in the manufacture of the integrated circuit device wherein said anti-reflective coating layer is a polishing stop.

10. (Previously Presented) The method according to Claim 9 wherein said first metal layer and said second metal layer comprise one of the group of: aluminum, aluminum alloys, tungsten and copper.

11. (Original) The method according to Claim 9 wherein said first metal layer is deposited to a thickness of between about 1,000 Angstroms and 10,000 Angstroms.

12. (Original) The method according to Claim 9 wherein said second metal layer is deposited to a thickness of between about 3,000 Angstroms and 10,000 Angstroms.

13. (Canceled)

14. (Canceled)

15. (Previously Presented) The method according to Claim 9 wherein said step of etching through said second metal layer to form vias has an endpoint at said etch stop layer.

16. (Canceled)

17. (Canceled)

18. (Previously Presented) A method of forming self-aligned, anti-via interconnects in an integrated circuit device comprising:

providing a semiconductor substrate;

depositing a first metal layer overlying said semiconductor substrate;

depositing an etch stop layer overlying said first metal layer wherein said etch stop layer comprises a tantalum containing film;

depositing a second metal layer overlying said first metal layer;

depositing an anti-reflective coating layer comprising titanium nitride (TiN) overlying said second metal layer;

etching through said anti-reflective coating layer, said second metal layer, said etch stop layer, and said second metal layer to form connective lines;

thereafter etching through said anti-reflective coating layer and said second metal layer to form vias wherein said etch stop layer acts as an etch stop;

thereafter depositing a dielectric layer overlying said vias, said connective lines and said semiconductor substrate wherein said dielectric layer is SiOF (fluorinated silica glass), SiOC (C-substituted siloxane), amorphous SiC:H, MSQ (methylsilsesquioxane), porous materials, PPXC polymer (poly(chloro-p-xylylene), PPXN polymer (poly-p-xylylene), or VT-4 (tetrafluoro-p-xylylene); and

polishing down said dielectric layer to complete said self-aligned, anti-via interconnects in the manufacture of the integrated circuit device wherein said anti-reflective coating layer is a polishing stop.

19. (Original) The method according to Claim 18 wherein said first metal layer and said second metal layer comprise one of the group of: aluminum, aluminum alloys, tungsten, and copper.

20. (Original) The method according to Claim 18 wherein said first metal layer is deposited to a thickness of between about 1,000 Angstroms and 10,000 Angstroms.

21. (Original) The method according to Claim 18 wherein said second metal layer is deposited to a thickness of between about 3,000 Angstroms and 10,000 Angstroms.

22. (Canceled)

23. (Canceled)